IN THE SPECIFICATION

Please replace the paragraph starting on page 4, line 6 with the following new paragraph:

Figure 1 is a circuit diagram illustrating of a memory unit illustrating the details of a memory array in one embodiment. ROM 100 is shown containing row decoder 160, column decoder 170, memory array 180 and [[multiplexor]] multiplexer 190. Merely for conciseness, memory array 180 is shown containing only 32 bit cells organized in the form of 2 rows, with each row containing 16 bit cells. The 32 bit cells are respectively implemented using 32 transistors 110-1 through 110-32. In the description below, the terms bit cell and transistor are used interchangeably.

Please replace the paragraph starting on page 4, line 13 with the following new paragraph:

Row decoder 160 receives 1-bit of a 5-bit address, and enables (sets to 1) one of word lines_101 and 102 depending on the value of the 1-bit. Column decoder 170 receives the remaining 4 bits and enables one of the 16 column select lines

190-1 through 190-16. As described below, the data stored in one of the 32 bit cells (corresponding to the value of the 5 bit address) is provided on path 199.

Please replace the paragraph starting on page 7, line 10 with the following new paragraph:

Diffusion layer 360 provides the source and drain areas for transistors 110-1 through 110-32. Poly-silicon layer 350 provides the gate area for_transistors 110-1 through 110-16, and poly-silicon layer 370 provides the gate area for transistors 110-17 through 110-32.